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EXAMINER

DICKEY, THOMAS L

ART UNIT PAPER NUMBER

2826

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/877,640

Applicant(s)

SMITH

Examiner

Thomas L Dickey

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pm

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-56,58-70,72-89,91,93-134 and 140-192 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) See Continuation Sheet is/are allowed.
- 6) ☒ Claim(s) 37,39-48,56,70,75,83,86,87,94-97,104,106-110,130-134,144-148,169,170 and 172 is/are rejected.
- 7) ☒ Claim(s) 88,89,91,93,98,105,173-175,179 and 180 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) filed 6/8/01 and 9/3/03
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims allowed are 26-36,38,49-55,58-69,72-74,76-82,84,85,99-103,111-129,140-143,149-168,176-178 and 181-192.

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DETAILED ACTION

1. The amendment filed on 01/14/2004 has been entered.

Information Disclosure Statement

2. The Information Disclosure Statements filed on 6/8/2001 and 9/3/2003 have been considered.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

A. Claims 37,47,56,70,75,83, and 130-134 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention, to wit: With regard to claim 37 the specification does not teach how to make a structure comprising an assemblage of separate electronic devices, each electronic device comprising a group II-VI compound and having a first surface and a second surface substantially parallel to said first surface, said electronic device further having side surfaces connecting said first surface to said second surface,

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said first surface having a smaller area than said second surface. Note that to do so requires etching, milling, or otherwise creating a block of group II-VI compound wherein different crystal planes of said group II-VI compound are exposed. With regard to claim 56 the specification does not teach how to make a shaped block of material comprising a group II-VI compound, adapted for being received in a recess of a substrate, said shaped block of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to said bottom surface, said top surface being non-congruent with said bottom surface. With regard to claim 75 the specification does not teach how to make a semiconductor microstructure comprising a shaped block having a first surface substantially parallel to a second surface, said first surface having an associated first area, said second surface having an associated second area, said first area being larger than said second area, an edge adjacent to said first surface being sloped, said block having a maximum length dimension less than or equal to 1 mm in measure, wherein said shaped block comprises a group II-VI compound. With regard to claim 83 the specification does not teach how to make a portion of an integrated circuit device comprising a shaped functional block having etched sides and comprising a group II-VI compound material and having etched sides and a length dimension less than or equal to 1 mm in measure. With regard to claims 130-134 the specification does not teach how to make a laser comprising a shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, as per claim 130, or an optical detector comprising a

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shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, said block of semiconductor material having a beveled edge adjacent a major surface thereof, as per claim 134.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 39,43,44, and 145 stand rejected under 35 U.S.C. 102(b) as being anticipated by TAI (4670770).

Tai discloses an electronic device 11-12-13-14-15 comprising semiconductor material 11 and having a tapered profile, said electronic device 11-12-13-14-15 having a dimension (5-15 microns, note column 3 line 24) less than or equal to 1 mm in measure and in fact being less than 50 microns, said electronic device 11-12-13-14-15 being separated from a substrate 21, wherein said semiconductor material is a group III-V compound, specifically, gallium arsenide. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

B. Claims 39-42,48, 86,104,106-109, 144, 146-148, and 172 stand rejected under 35 U.S.C. 102(b) as being anticipated by NG et al. (H208).

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(1) With regard to claims 39-42, 48, 144, and 146-148, Ng et al. discloses an electronic device 14 comprising multilayered semiconductor material and having a tapered profile, said electronic device 14 having a dimension (the depth of the block being .25-.75 mm) less than or equal to 1 mm in measure and in fact less than or equal to 500 microns, said electronic device 14 being separated from a substrate 10, further having a first (top) surface and a second (bottom) surface substantially parallel to said first surface, wherein the perimeter of said first surface has a rectangular shape, an octagonal shape, or a circular shape, a cross-section thereof shows one of a cylindrical shape, a rectangular shape, a square shape, a hexagonal shape, a T-shape, and a kidney shape, said profile has a trapezoidal shape and at least a partially beveled edge, and wherein the electronic device 14 has one of a pyramid shape and a truncated pyramid shape. Note figures 4-7 and column 3 lines 2-3 and column 4 lines 12-19 and 33-35 of Ng et al.

(2) With regard to claims 86 and 172, Ng et al. discloses a electronic chip comprising a block of material 14 separated from a substrate 21 and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areal measurement larger than an areal measurement of said second surface, said first surface having a conductive contact 16 disposed thereon, wherein said shaped block has an inwardly sloped

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profile. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al.

(3) With regard to claims 104 and 106-109, Ng et al. discloses a electronic component 14 separated from a first substrate 21 comprising a first (bottom) surface; a conductive contact 16 disposed atop said first surface; a second surface (top) in substantially parallel relation to said first surface and having a smaller surface than said first (bottom) surface; and etched (side) surfaces connecting said first surface to said second surface, said etched surfaces being tapered to define at least a beveled edge to said first surface, wherein said electronic component 14 is adapted for self-alignment within a shaped opening through a surface of a second substrate, should such a second substrate present itself. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al.

The applicant's claims 106-109 do not distinguish over the Ng et al. reference regardless of the process used to form said etched surfaces, because only the final product is relevant, not the recited processes of wet etching, mask edging, reactive ion etching, or ion milling. It is noted that these processes are exclusive alternates, only one may be used. Since applicant claims that any of them may make the claimed invention, it is impossible for any single one of them to leave a distinguishing mark on the claimed invention, unless somehow all of them leave

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that mark. As noted below, case law assigns applicant the burden of showing how such a mark is left.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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A. Claims 45,46,94-97, and 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over NG et al. (H208) in view of FANG et al. (IBM Technical Disclosure, vol. 19, No. 10, Mar. 1977, pp. 3959-3960).

(1) Ng et al. discloses an electronic device comprising semiconductor material and separated from a substrate, having all the limitations of claims 45 and 46 except that said semiconductor material is a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al. However, Fang et al. discloses an electronic device comprising semiconductor material 2-3-4-7-8 and separated from a substrate 10, with a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic device comprising semiconductor material and separated from a substrate with the light-emitting diode, specifically the gallium arsenide light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(2) Ng et al. discloses an electronic chip comprising a block of material separated from a substrate, having all the limitations of claims 94-97 except that said electronic chip is a light-emitting diode or a gallium arsenide diode, specifically a

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gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al. However, Fang et al. discloses an electronic chip comprising a block of material 2-3-4-7-8 separated from a substrate 10, with a light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic chip comprising a block of material separated from a substrate with the light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(3) Ng et al. discloses an electronic component separated from a first substrate, having all the limitations of claim 110 except that the electronic component is a light-emitting diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al. However, Fang et al. discloses an electronic component 2-3-4-7-8 separated from a first substrate 10, with a light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic component

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separated from a first substrate with the light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

B. Claims 87, 169, and 170 stand rejected under 35 U.S.C. 103(a) as being unpatentable over NG et al. (H208) in view of GARDNER et al. (5055892).

Ng et al. discloses an electronic chip comprising a block of material having all the limitations of claims 169, 170, and 87 except that said block of material has a width of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87) and a length of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87). Note the explanation regarding claim 86 in section 7B above. Ng et al. does not disclose the 50-micron to 1 mm scale for the block of material as claimed by the applicant.

Gardner et al. discloses a device with a block of material, being in Gardner et al.'s version a functioning LED, having typical dimensions of 250 microns length, breadth, and depth. Note column 6 lines 25-26 Gardner et al. Therefore, it would have been obvious to a person having skill in the art to scale Ng et al.'s block of material in the ranges 50 microns to 1 mm, such as taught by Gardner et al. in order to build the block of material in the scale ranges typically known to the art at the time of the invention. Although neither Gardner et al. nor Ng et al. disclose the 50 micron scale for the block of material it has recently been observed that a *prima facie* case of obviousness

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typically exists when the ranges of a component of the claimed invention overlap the ranges disclosed in the prior art or when the ranges of the component do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003). It appears that in this case, one skilled in the art would have expected a 50 micron block of material to have the same properties as the 250 micron block of material disclosed by Gardner et al.

Allowable Subject Matter

6. The following claims have been found allowable:

A. Claims 26-36,38 and 140-143 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a structure comprising an assemblage of separate electronic devices, each electronic device having a first surface and a second surface substantially parallel to said first surface, said electronic device further having a beveled side connecting said first surface to said second surface, said first surface having a smaller area than said second surface, said electronic device further having electronic structures formed on said second surface, as recited in claim 26.

B. Claims 49-55, 58 and 149-153 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a shaped block of material adapted for being received in a recess of a

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substrate, said shaped block of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to said bottom surface, said top surface being non-congruent with said bottom surface, a larger of said top surface and said bottom surface having formed thereon an electronic device, as recited in claim 49.

C. Claims 59-69 and 154-158 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a shaped functional block comprising a semiconductor material and having a shape adapted for self-alignment within a shaped recess formed through a substrate surface, said block having a first surface and a second surface and having etched sides which are sloped such that said block fits into said shaped opening; only in an orientation where said first surface is exposed through said substrate surface, said first surface connected to said second surface only by said etched sides, said first surface being larger than said second surface and having electronic structures formed thereon, as recited in claim 59.

D. Claims 72-74 and 76-78 and 159-163 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor microstructure comprising a shaped block having a first surface substantially parallel to a second surface, said first surface having an associated first area, said second surface having an associated second area, said first area being larger than said second area, an edge that is adjacent to both said first and

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second surfaces, said second surface being sloped, said first surface having formed thereon electronic structures, said block having a maximum length dimension less than or equal to 1 mm in measure, as recited in claim 72.

E. Claims 79-82,84,85 and 164-168 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a portion of an integrated circuit device comprising a shaped functional block, said functional block comprising a semiconductor material and having a length dimension less than or equal to 1 mm in measure, said functional block having a top surface, a bottom surface that is smaller than said top surface, and etched sides that connect said top surface to said bottom surface, said top surface having formed thereon an electronic device, as recited in claim 79.

F. Claims 99-103 and 176-178 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an electronic chip comprising a shaped functional block including a semiconductor material, said functional block having tapered sides connecting a top surface to a bottom surface smaller than said top surface, said top surface having formed thereon at least one electronic device, said functional block further having a length dimension less than or equal to 1 mm in measure, a perimeter of said top surface having a rectilinear shape, a circular shape, or an octagonal shape, as recited in claim 99.

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G. Claims 111-117 and 181-182 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a light-emitting diode (LED) comprising a shaped semiconductor block having tapered sides, said semiconductor block comprising a first surface and a second surface in substantially parallel relation to said first surface, said tapered sides being tapered to define at least a beveled edge to both first and second surfaces, said first surface being larger than said second surface and having formed on said first surface an electronic structure for producing light, as recited in claim 111.

H. Claims 118-122 and 183-185 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a light-emitting diode (LED) comprising an amount of semiconductor material, said semiconductor material having a first surface and a second surface smaller than said first surface, said semiconductor material having non-parallel side surfaces connecting said first surface to said second surface, said LED having a length dimension less than or equal to 1 mm in measure, said first surface having formed thereon an electronic structure for producing light, as recited in claim 118.

I. Claims 123-129 and 186-188 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a light-emitting diode (LED) comprising a block of semiconductor material including gallium arsenide, said block having a top surface and a bottom surface smaller in area than said top surface connected to said top surface by sloped surfaces, said

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block having length dimension less than or equal to 1 mm in measure, said top surface having layers formed thereon to produce light, as recited in claim 123.

J. Claims 189-192 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a shaped block of semiconductor material having tapered sides, said block of material comprising a first surface and a second surface in substantially parallel relation to said first surface and smaller in area than said first surface, said tapered sides defining a beveled edge adjacent both said first and second surfaces, said first surface having formed thereon an electronic device, as recited in claim 189.

Pogge et al. 5,770,884, filed 6/30/1995, discloses (but does not claim) all the elements of claims 26,49,59,72,79,99,111, and 189. Note figures 2G, 2G', 6A, 8C, and accompanying text in Pogge et al. However, it has been determined that claims 26,49,59,72,79,99,111, and 189 are fully disclosed and enabled in the disclosure of parent application 08/480,500 filed 6/7/1995. For this reason claims 26, 49, 59, 72, 79, 99, 111, and 189 are entitled to an effective filing date not later than 6/7/1995, rendering Pogge et al. 5,770,884 ineffective.

Claims 88,89,91,93,98,105,171,173-175,179, and 180 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Response to Arguments

7. Applicant's arguments filed 01/14/04 have been fully considered but they are not persuasive.

It is argued, at page 22 of the remarks, that "It is settled law that an inventor is not required to disclose every detail of the invention, only enough that would allow one of ordinary skill in the art to use and practice the invention. It is respectfully submitted that the disclosed alternate materials, including group II-VI compounds, are within the scope of knowledge of one of ordinary skill in the art to which the present invention pertains." However, the settled law applicant refers to specifically requires a factual showing that one of ordinary skill in the art would have been able to use and practice the invention as of the effective filing date of the application. Further, the settled law applicant refers to requires that the entire scope of the claim be enabled at that time. The examiner has searched in vain for a reference published on or before 06/07/1995 (the effective filing date of the instant application) teaching one how to machine any and all II-VI materials with the bevels, planes, and tapers required to meet claims 37,56,75,83. If applicant is aware of such a reference he is asked to please help the examiner make it of record.

It is argued, at page 21 of the remarks, that "Claims 47, 70, and 130-134 have been amended to recite a laser." However, while this amendment solves the written description problem in a quite literal sense, it compounds the enablement problem. As discussed above, settled law requires that the entire scope of the claim be enabled as of the effective date. The examiner is of the belief that one of ordinary skill in the art on

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6/7/95 might have practiced applicant's invention using, for example, the half-wave Bragg reflector VCSEL of Kahen 5,212,703, published 5/18/1993. However, the scope of amended claims 47, 70, and 130-134 (unfortunately the narrowest scope supported by applicant's parent filing) is far broader than that.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Mon-Thu 8-6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn

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can be reached on 571-272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
04/2004


Minhloan Tran
Primary Examiner
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